An Embedded 12-bit 80MS/s A/D/A Interface for Power-Line Communications in 0.13μm Pure Digital CMOS Technology

Manuel Delgado-Restituto, Jesús Ruiz-Amaya, José M. de la Rosa, Juan F. Fernández-Bootello, Leila Díez, Rocío del Río and Ángel Rodríguez-Vázquez

Instituto de Microelectónica de Sevilla, Centro Nacional de Microelectrónica
Avda. Reina Mercedes s/n, 41012-Sevilla (SPAIN), Tel: +34 - 95 505 6666
E-mails: Manuel.Delgado@imse.cnm.es

***Abstract*— This paper presents an embedded interface, comprising both A/D and D/A converters, which has been implemented in a 0.13μm pure digital CMOS technology. The interface is integrated in a system for high-performance broad-band power-line communications. The A/D converter uses a pipelined structure, whereas the D/A stage is based on segmented current steering techniques. In both cases, specifications are 12-b resolution at 80MS/s and MTPR above 56dB.**

***Index Terms*— Data Converters, Embedded Converters, Pipeline A/D Converters, Current-Steering D/A Converters.**[1]

I. INTRODUCTION

Apart from relying on the low-level physics of the fabrication process, as any mixed-signal circuit, embedded data converters (i.e., converters which share the semiconductor substrate with a large, often multi-million transistor, digital circuitry) present some difficulties which further complicate their design. Most important, they can be seriously affected by the digital switching activity running in the common substrate and so, additional considerations and techniques must be applied to reduce the substrate and supply noise couplings, which otherwise would degrade converter' performance [1]-[3]. This mixed-signal integrity problem becomes more acute as the sampling rate and dynamic range specifications for data converters increase, as it is the trend in modern communication applications. Additionally, economical reasons often dictate that the whole system integration is realized in low-suited pure-digital CMOS technologies. In these cases, embedded converters cannot use specific analog-oriented structures for resistors and capacitors (e.g., MIM sandwiches), and designers must rely to less efficient passive structures in terms of linearity, parasitics or area consumption.

In this paper, the design of a conversion interface, comprising both A/D and D/A converters, embedded in a system for broad-band power-line communication is described. It has been designed in a 0.13μm 1-poly 8-metal logic CMOS process and features high-speed and high-linearity specifications for both the A/D and D/A stages; namely, 12-b resolution at a sampling rate of 80MS/s and Multi-Tone Power Ratio (*MTPR*) above 56dB from a nominal 3.3V analog power supply. The designs are also compliant with industrial operation conditions as of temperature (-40 to +85º C) and supply (±10%) variation ranges. There are excellent contributions in the literature that meet these (and even more demanding) specifications (see, for instance, [4], [5]), but the challenging aspect of the presented designs is to accomplish them in a noisy embedded environment and with a non analog-oriented technology.

Given the high-speed requirements, Nyquist-rate solutions has been adopted for both converters; a pipelined structure for the ADC, and a segmented current-steering topology for the DAC. Section. II describes the architectural and circuit techniques used in the design of the pipelined converter, whereas Section. III gives details on the design of the current-steering DAC. Section. IV presents simulation results of both converters, and Section. V concludes the paper.

II. PIPELINED A/D CONVERTER

A. Architectural Considerations

The block diagram of the proposed 12-bit A/D converter is shown in Fig. 1 It consists of a 9-stage pipelined structure, preceded by a sample/hold (S/H) amplifier (to ensure good undersampling performance) and terminated by a 2-b flash sub-ADC. Each stage provides 1.5 effective bits, except for the first one, which obtains 2.5 effective bits to improve the linearity of the ADC and reduce the accuracy requirements on subsequent stages [6]. The MDACs of all the pipelined stages use conventional fully differential topologies based on switched-capacitor techniques [6]. Fig. 2 shows, for illustration purposes, the block diagram of the MDACs used for the 1.5-b stages ($j = 2, \ldots 9$). The S/H amplifier implements a flip-around topology for noise and power reduction [4]. Redundant Signed Digit (RSD) coding is used in all the flash sub-ADCs, except the final one, in order to reduce the resolution requirements of their comparators, and thereafter, their power consumption. A Digital Correction Logic (DCL) block, which includes delay equalizing registers, digital adders, and an ADC overload detector, is used to compensate for comparator errors and synthesize the 12-b digital output data. A clock generator circuit externally driven by a 160MHz reference (and internally divided by two in frequency) is used to synthesize the two non-overlapping clock phases (Φ_{1D} and Φ_{2D}) for the concurrent operation of all the stages. The clock generator also provides two slightly shorter phases (Φ_1 and Φ_2) to prevent signal dependent charge injection in the MDAC's [6] (see Fig. 2). Other extra supporting circuits included in the design are a precision bandgap

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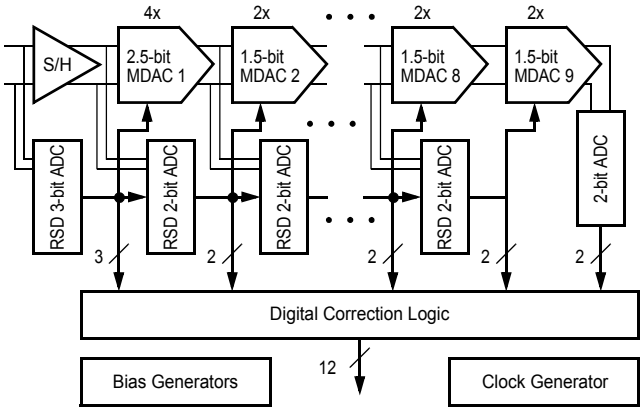
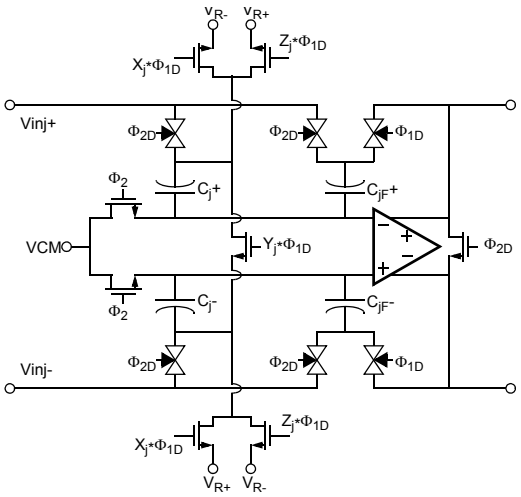
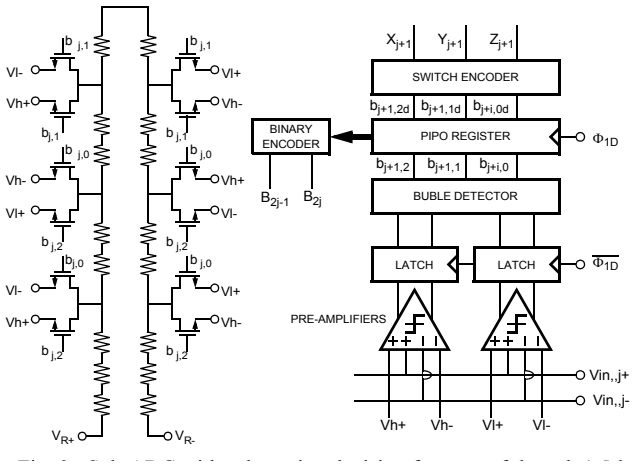


Fig. 1. 12-b ADC Block Diagram.





network, a differential reference buffer to define the full scale conversion range, and an additional buffer to set the common-mode voltage of the MDAC's. The pipelined converter uses no calibration or dithering circuitry.

Two major architectural solutions have been adopted for the sake of power reduction: dynamic reference selection and scaling down the pipelined toward its backend. The objective of dynamic reference selection [7] (also called subranging reference voltage switching [8]), is to anticipate the (signal dependent) digital control signals of the MDAC (signals X_j, Y_j and Z_j in Fig. 2) by a half a clock cycle, so that the time required by the sub-ADC comparators to make a decision do not fall into the amplification phase of the MDACs. In this way, both the MDAC´s and the sub-ADCs have a complete half cycle for settling (no racing conflict exists) and their corresponding power consumptions can be reduced. The price is a slightly more complicated sub-ADC structure because of the subranging reference selection [7]. Fig. 3 shows an example of sub-ADC for the (j+1)-th 1.5-b stage of the pipelined architecture. As can be seen, decision control signals X_{j+1}, Y_{j+1} and Z_{j+1} are obtained from comparator decisions ($b_{j,0}$, $b_{j,1}$ and $b_{j,2}$) obtained from the previous j-th 1.5-b stage one clock cycle earlier.

Because the required resolution of the stages decreases towards the backend of the pipeline structure, there is the possibility of scaling the integrating capacitor values, switches and amplifiers in order to reduce the overall power consumption of the pipeline. In our design, we have adopted a compromise between design complexity and power saving by designing five different amplifiers, whose requirements on linearity and speed are progressively relaxed down the ADC architecture. Table 1 shows the minimum specifications for these operational amplifiers used in pipeline. Similarly, four different integrating capacitors with reduced capacitance values are employed. Thanks to this scaling technique, the power consumption is progressively decreased since the first stage to the last one, as indicated in Fig. 4.

B. Circuit Design

The pipelined converter has been designed in a 0.13µm 1-poly 8-metal logic CMOS process. Analog blocks in Fig. 1 have been implemented with thick-oxide transistors (with a minimum feature size

Table 1: Operational amplifier' specifications

Operational amplifier	S	A	B	C	D
Stages	S/H	1	2-3	4-6	7-9
Maximum Equivalent load (pF)	9.6	29.6	10.2	7.95	7.95
Minimum Slew-Rate (V/µs)	500	301	310	212	101
Minimum GBW (MHz)	265	240	246	169	76
Minimum DC-gain (dB)	55	74.8	68	60	54
Eq. inp. noise PSD ($nV/\sqrt{Hz}$)	<3	<3	<5	<30	<140

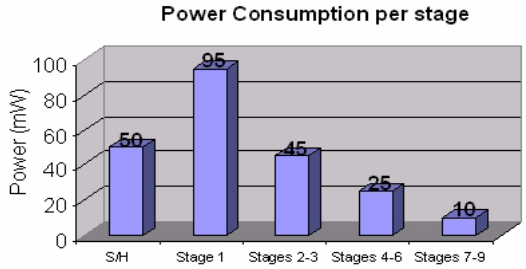


Fig. 4. Power consumption per stage after amplifier and integrating capacitor scaling.

of 0.34μm), whereas digital blocks (clock generator and DCL) use thin-oxide devices, in order to reduce croostalk effects and the overall power consumption. The interface between them is accomplished by high-speed robust level shifters.

The pipelined ADC uses substrate biased MOSFETs operated in the depletion region as capacitors, and employs series compensation techniques [9] to improve their linearity, as shown in Fig. 5. These capacitors offer good matching properties (enough for the required 12-b of the ADC) and linearity (the dominant second order nonlinear coefficient is about 0.125%/V in a 3pF implementation [9]), and obtains a capacitance per unit area of 0.4fF/μm^2. Unfortunately, they also show large parasitic capacitances, xwhat explains the large equivalent load of amplifiers in Table 1.

Fig. 6 shows the schematic of the operational amplifiers used for both the S/H amplifier and the first six pipelined stages (the last three stages use conventional PMOS input folded-cascode topologies). It is a fully differential two stage design with a telescopic cascode input stage and a differential output stage. Capacitors for (double cascode) compensation are made of multiplate sandwich structures. Note that p-type input schemes has been preferred, the main reason being the possibility to cancelling the body effect in the PMOS devices – one of the mechanism for substrate noise coupling [1]-[3]. The design approach for other circuit elements in Fig. 1 and 2 (e.g., flash sub-ADC and switches) can be found in [10].

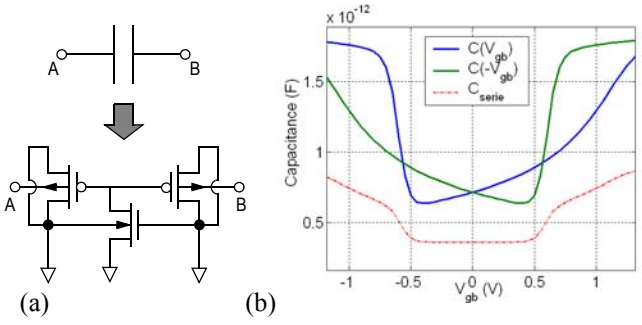


Fig. 5. (a) Capacitor implementation by substrate biased depletion-mode PMOS transistors in series compensation. (b) Illustration of the capacitance linearization principle.

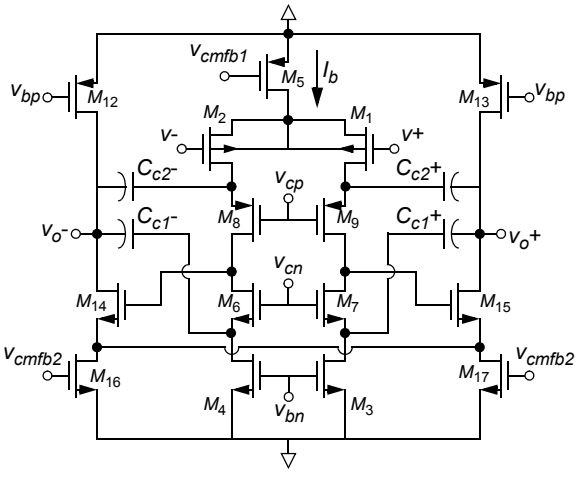


Fig. 6. Schematic of the operational amplifier used in the first six stages of the pipelined ADC and the input S/H amplifier.

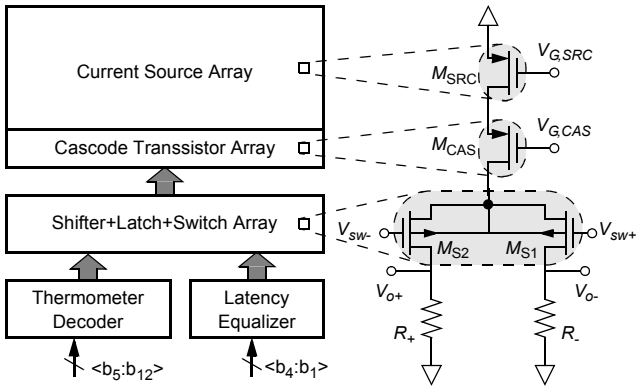


Fig. 7. Basic block diagram of the Current Steering converter.

III. CURRENT-STEERING D/A CONVERTER

The basic block diagram of the current-steering converter is illustrated in Fig.7. The converter has a segmented architecture with 4 binary bits and 8 thermometer bits which guarantees a good accuracy-active area trade-off [11], [12]. The basic current cell is composed of a PMOS current source transistor (CS), a PMOS cascode transistor (CAS) and two complementary PMOS switch transistors (SW and $\overline{\text{SW}}$), driven with reduced swing control signals generated by a level-shifter+latch+driver circuit. Special attention has been taken on critical aspects of the current cell, such as finite output impedance, glitches, clock-feedthrough and matching.

In order to reduce systematic gradient errors, the Q^2 Random Walk switching sequence proposed in [13] has been selected. Also, the unary current source array has been split up in a double common-centroid layout distribution for improving tolerance to random gradient errors.

The thermometer decoder has been synthesized using commercial synthesis tools from a VHDL functional description based in the decoder presented in [14].

IV. SIMULATION RESULTS

At this point, both the ADC and DAC converters are being laid out for fabrication. All major layout techniques to deal with substrate coupling effects are being considered [1]-[3]. It is expected that measured results will be available at the Symposium. Hence, only simulation results will be shown in this section.

Fig.8 shows the output spectra of the ADC [Fig.8(a)] and DAC [Fig.8(b)] for a 38 MHz input signal, close to the Nyquist frequency of the converters. In the first case, the SNR is 64dB and the SNDR is 62dB. For the DAC, corresponding metrics are 71dB and 69dB.

Fig.9 show the output spectra of both converters for a digital multi-tone (DMT) input signal consisting of 1536 tones distributed from 4.3MHz to 34MHz, where 16 consecutive tones of have been suppressdd from each 256 sub-groups. The MTPR is better than 57dB in the ADC case [Fig.9(a)], and above 59dB for the DAC [Fig.9(a)], thus meeting the specifications on linearity.

The performance of the converters are summarized in Table 2 and 3, respectively. These results have been validated with monte-carlo analysis for all process corners assumming variations of -40º to 85ºC in temperature and 3V to 3.6V in power supply.

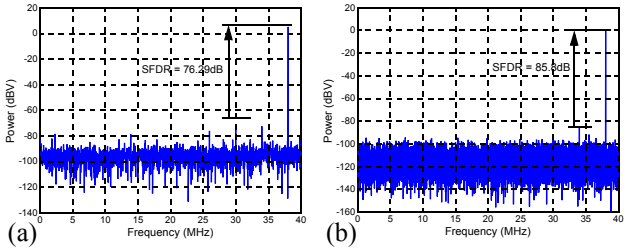


Fig. 8. Output spectra for a 38MHz input tone signal of the: (a) ADC and (b) DAC converter.

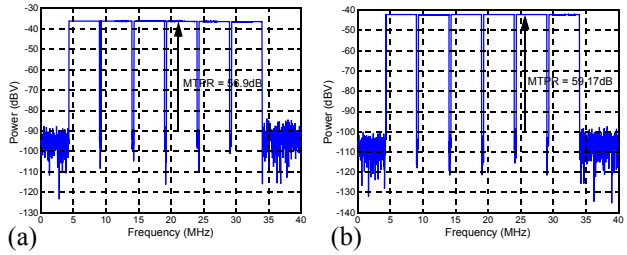


Fig. 9. Output spectra for a 240 tones on, 16 tones off DMT input signal of the: (a) ADC and (b) DAC converter.

V. CONCLUSIONS

This paper describes the design of an embedded interface, comprising both A/D and D/A converters, which has been implemented in a 0.13µm pure digital CMOS technology. In both cases, the converters achieve 12-b resolution at a sampling rate of 80MS/s and Multi-Tone Power Ratio (MTPR) above 56dB from a nominal 3.3V analog power supply.

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Table 2: Performance summary of the ADC

Resolution		12 bits
Conversion rate		80 MSPS
Input range		2.0 Vpp differential
SNR @ Nyquist		64 dB
SNDR @ Nyquist		62 dB
DNL @ 10 bits		<0.47 LSB
INL@ 10 bits		<0.57 LSB
MTPR	1 OFF-15 ON 8 OFF-120 ON 16 OFF-240 ON	57.13dB 57.07dB 57.25dB
Estimated power (3.3V analog supply)		390 mW

Table 3: Performance summary of the DAC

Resolution		12 bits
Conversion rate		80 MSPS
Output range (25Ω termination)		1.0 Vpp differential
SNR @ Nyquist		71 dB
SNDR @ Nyquist		69 dB
DNL @ 12 bits		<0.4 LSB
INL @ 12 bits		<0.5 LSB
MTPR	1 OFF-15 ON 8 OFF-120 ON 16 OFF-240 ON	60.22dB 59.27dB 59.16dB
Estimated power (3.3V analog supply)		125 mW

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